

FIGURE 1

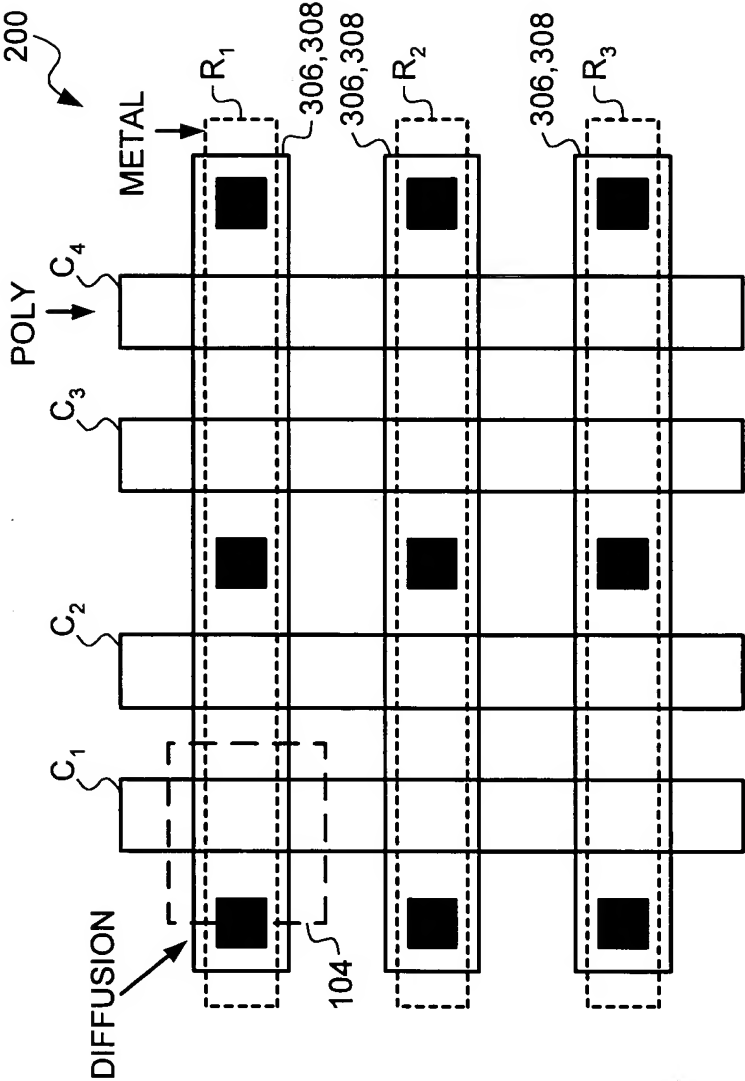


FIGURE 2

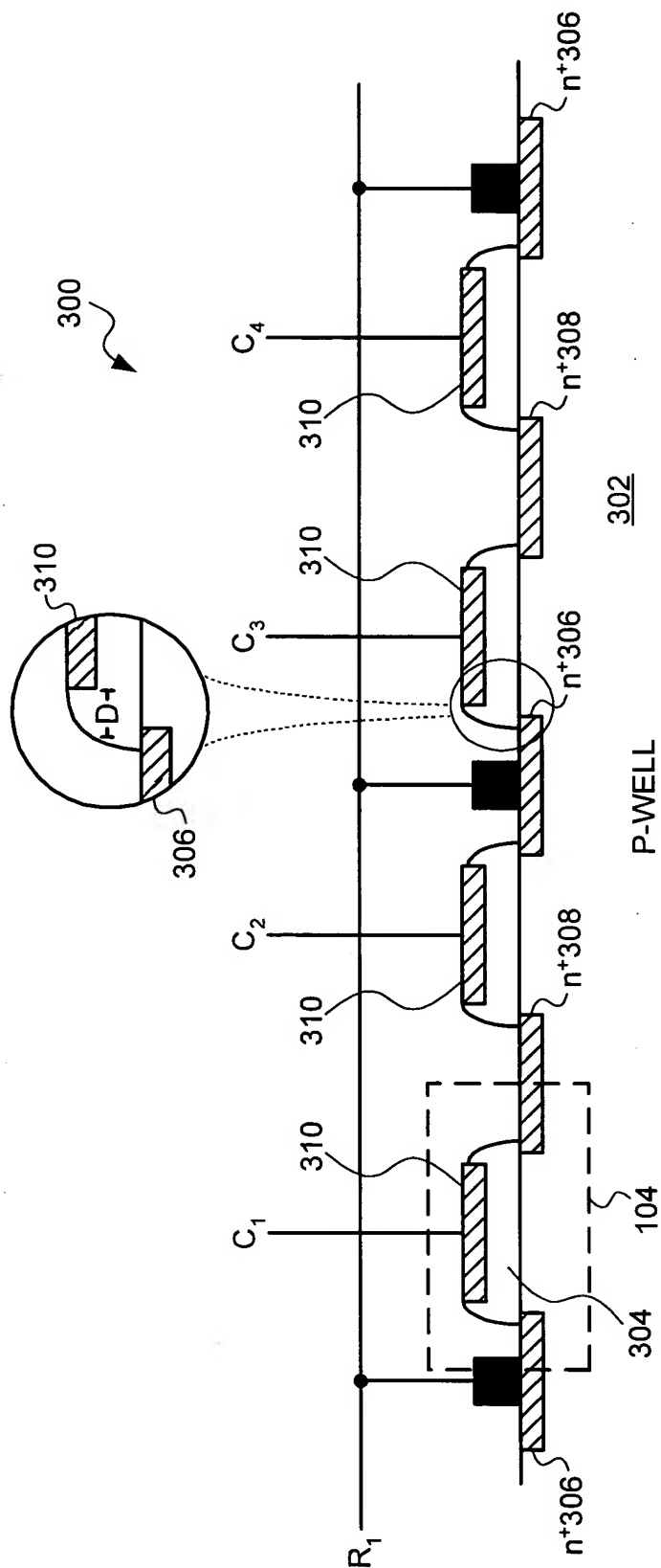


FIGURE 3

		VBL (V)	VWL (V)	PROGRAM	
PROGRAM	SC/SR	8	0	YES	401
	SC/UR	8	8	NO	403
	UC/SR	3.3	0	NO	405
	UC/UR	3.3	8	NO	407
				ISENSE	
READ	SC/SR	1.8	0	YES	409
	SC/UR	1.8	1.8	NO	411
	UC/SR	0	0	NO	413
	UC/UR	0	1.8	NO	415

FIGURE 4

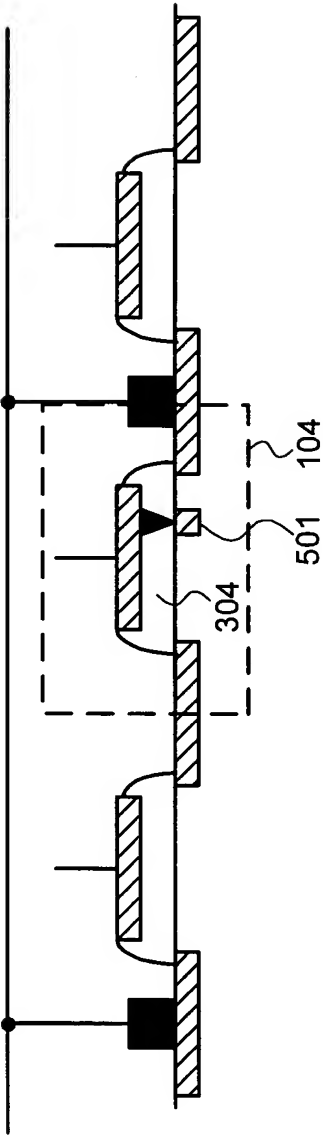


FIGURE 5

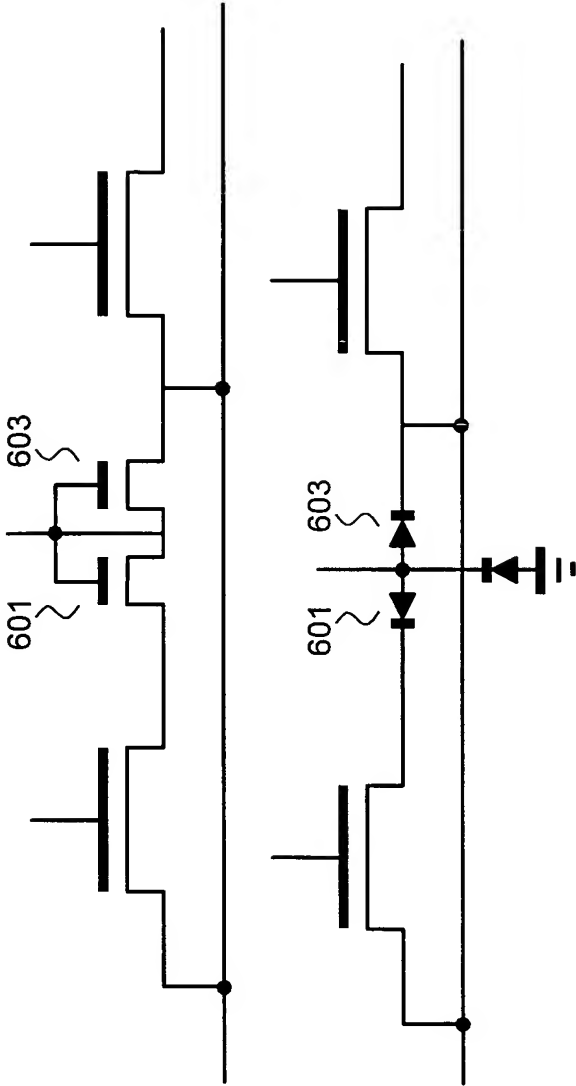
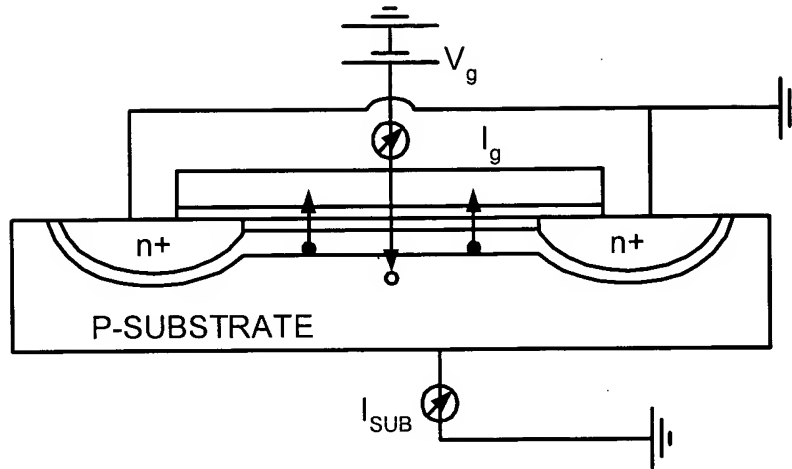
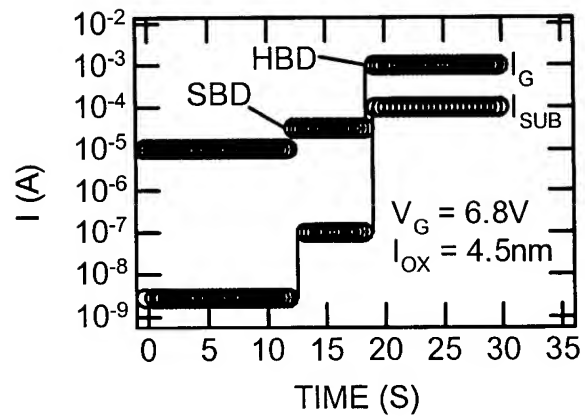
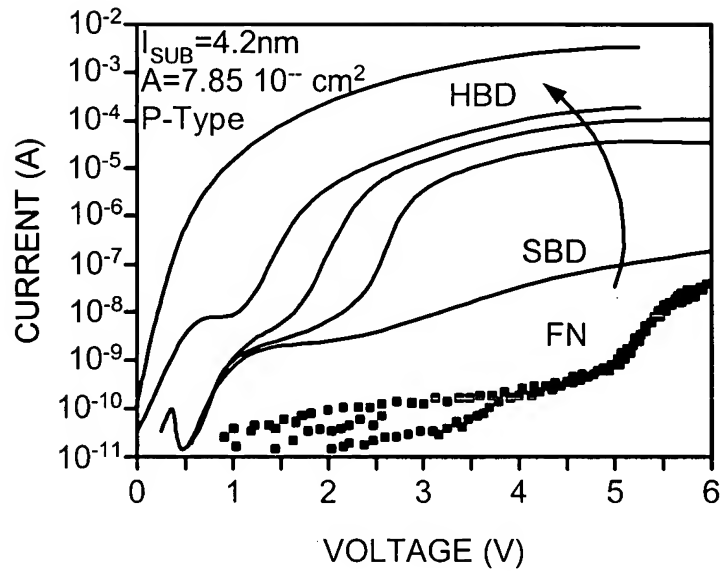


FIGURE 6

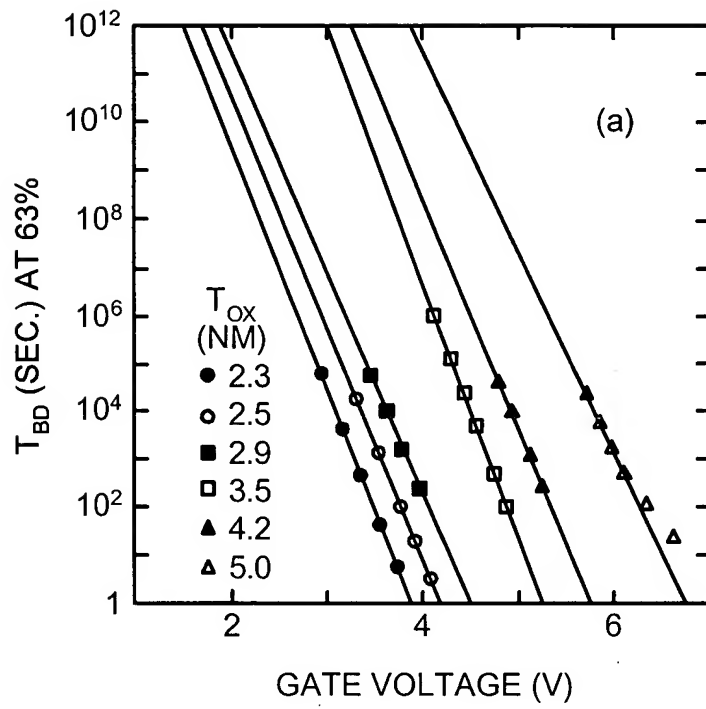
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**FIGURE 7****FIGURE 8**

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**FIGURE 9**

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**FIGURE 10**

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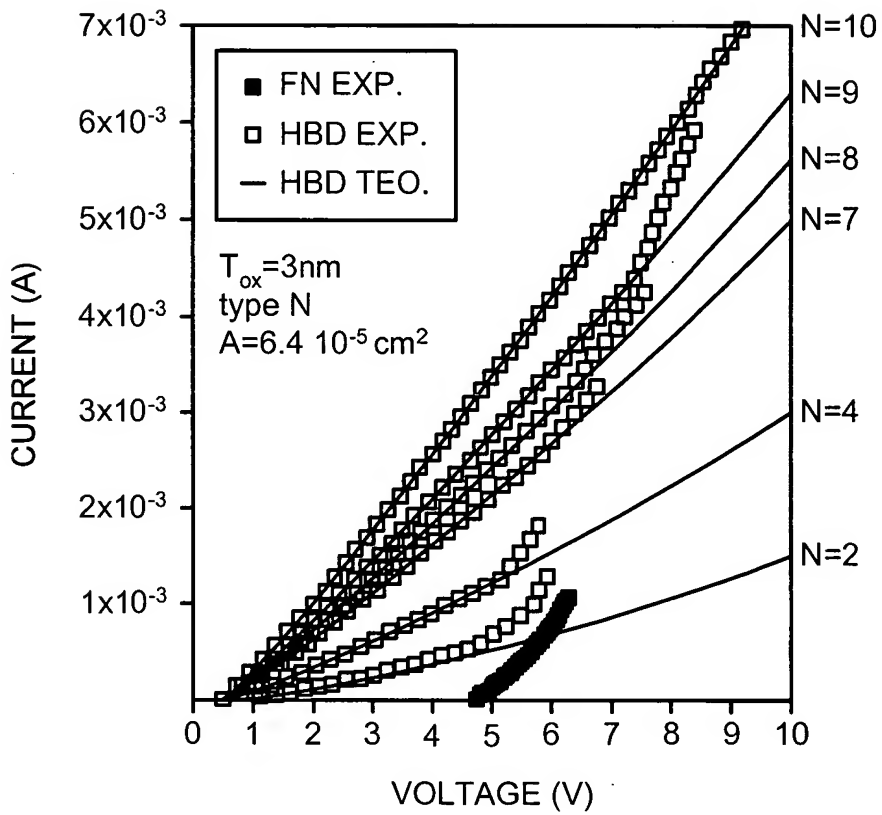


FIGURE 11

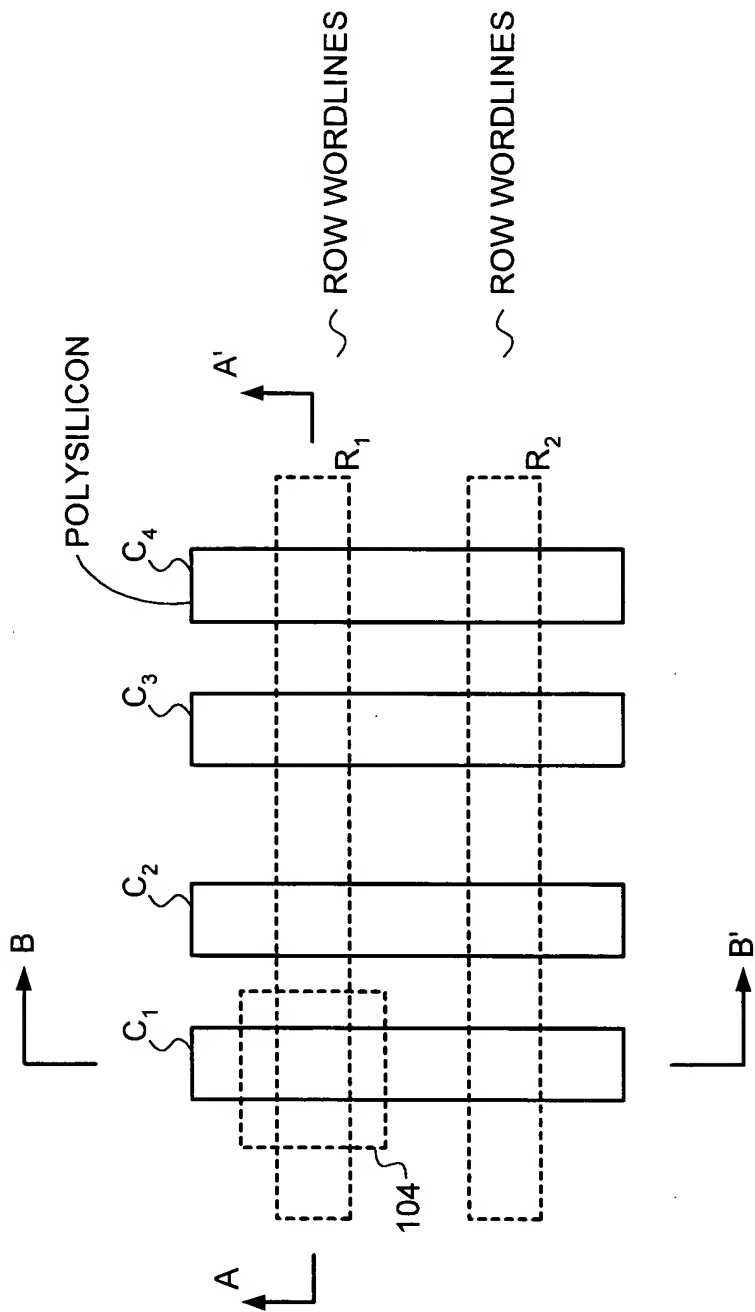
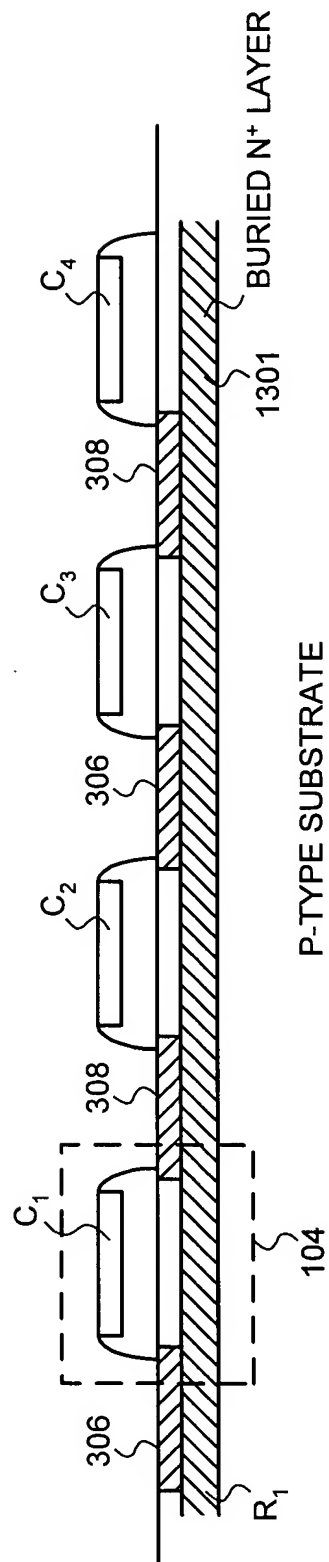


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**FIGURE 13**

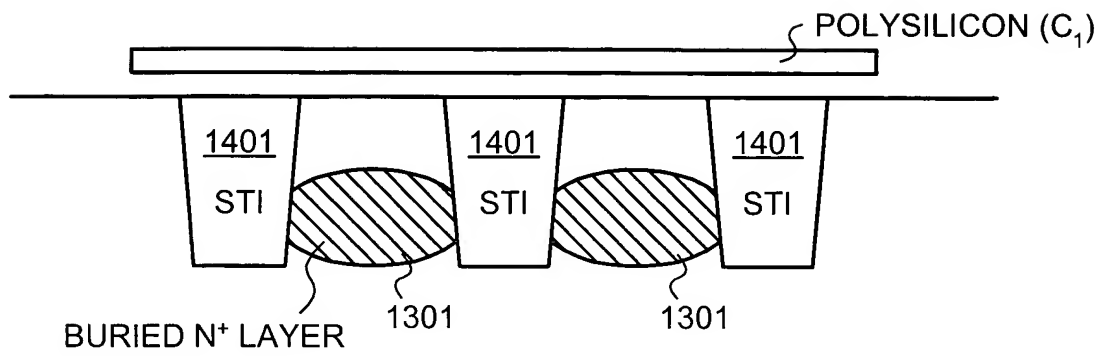
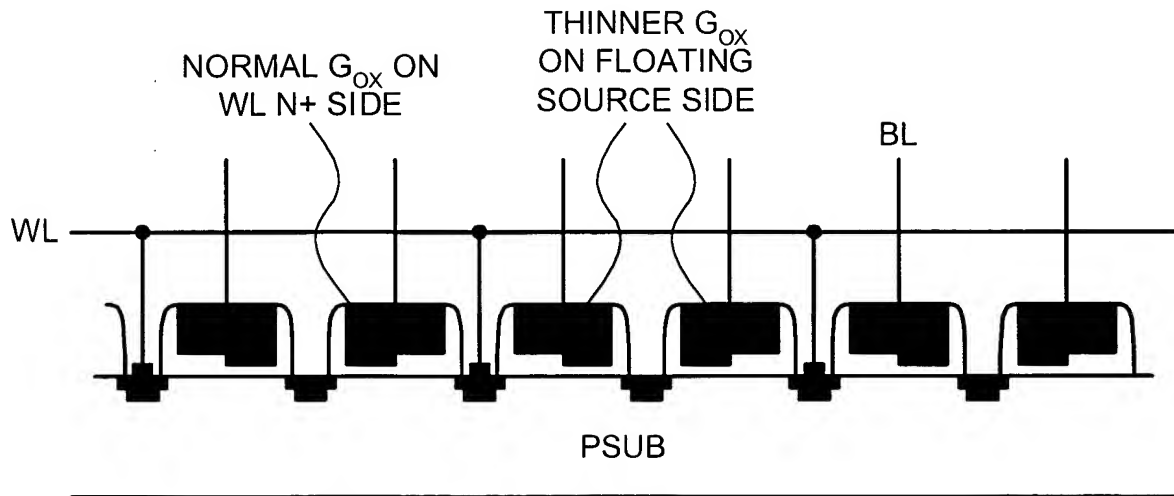
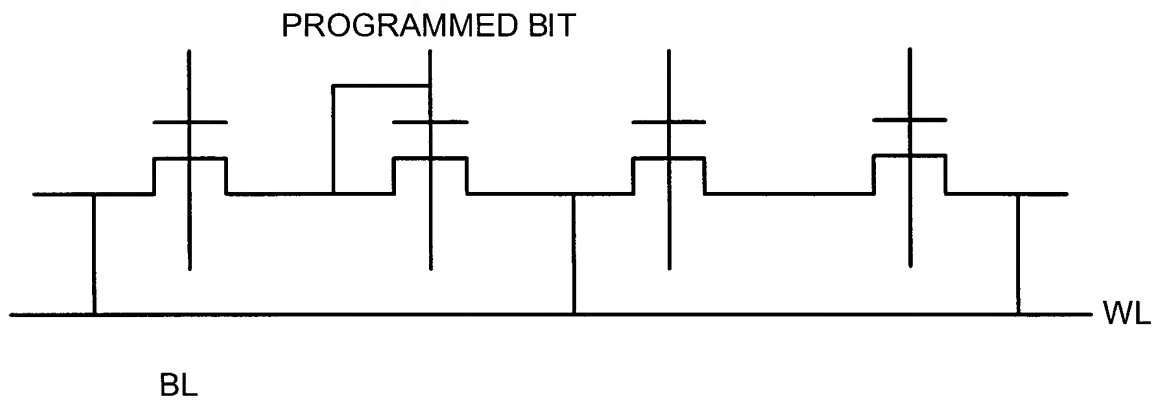


FIGURE 14

		VBL (V)	VWL (V)	PROGRAM	
PROGRAM	SC/SR	V _{PP}	0	YES	401
	SC/UR	V _{PP}	FLOATING	NO	403
	UC/SR	< 0.5 V	0	NO	405
	UC/UR	< 0.5 V	FLOATING	NO	407
READ				I _{SENSE}	409
	SC/SR	V _{DD} OR V _{CC}	0	YES	411
	SC/UR	V _{DD} OR V _{CC}	V _{DD} OR V _{CC}	NO	413
	UC/SR	0 OR FLOAT	0	NO	415
	UC/UR	0 OR FLOAT	V _{DD} OR V _{CC}	NO	

FIGURE 15

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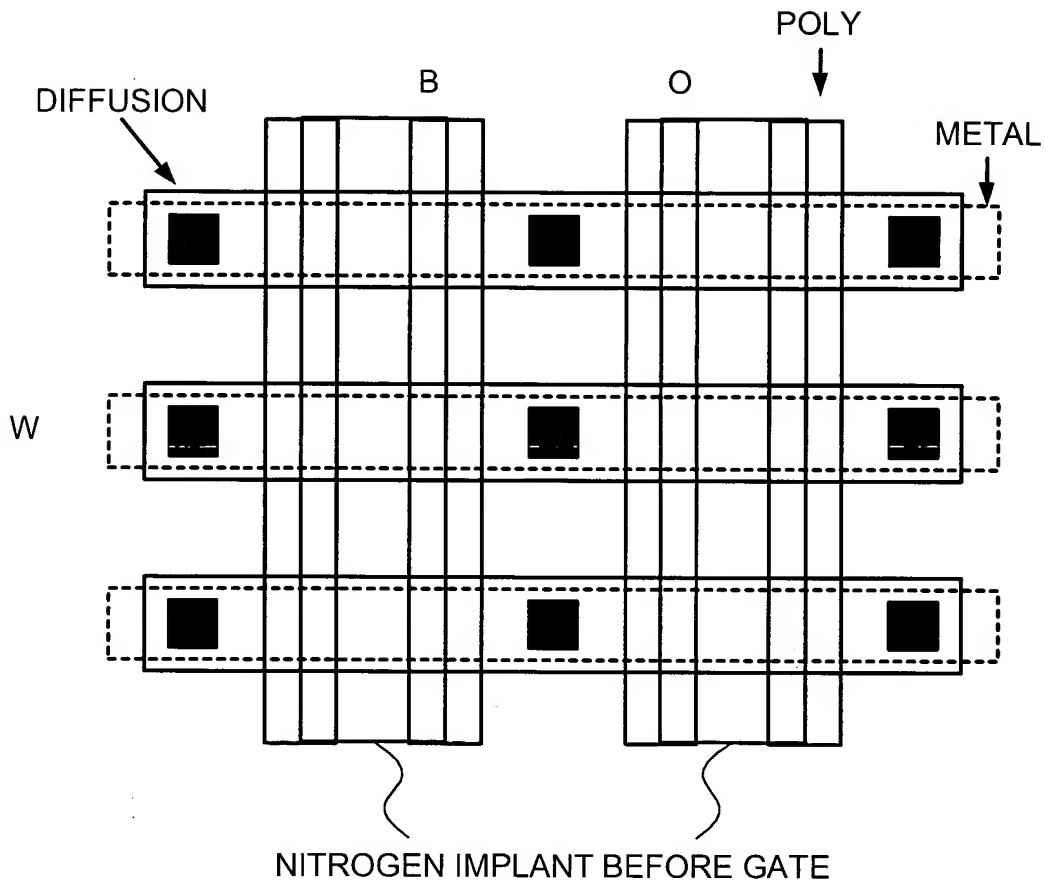
**FIGURE 16****FIGURE 17**

0.18um/0.13um XPM CX CELL OPERATION

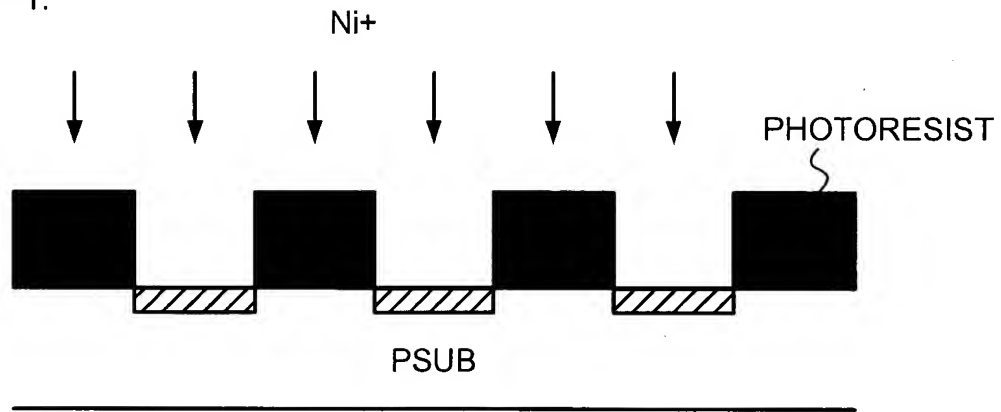
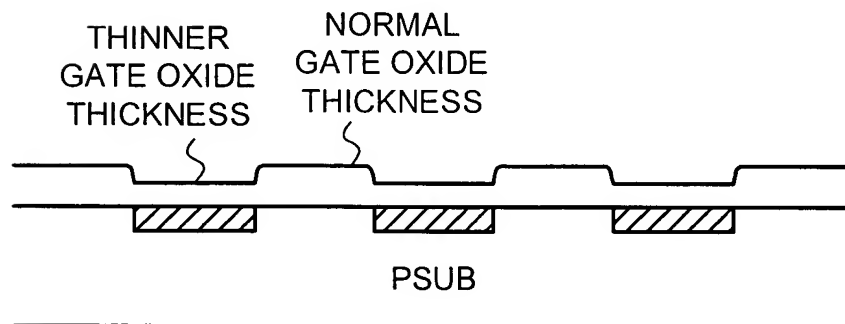
		VBL (V)	VWL (V)	PROGRAM
PROGRAM	SB/SW	V _{PP}	0	YES
	SB/UW	V _{PP}	PC TO V _{PP} /2 AND FL	NO
	UB/SW	< 0.5 V	0	NO
	UB/UW	< 0.5 V	PC TO V _{PP} /2 AND FL	NO
				I _{SENSE}
READ	SB/SW	V _{DD} OR V _{CC}	0	YES
	SB/UW	V _{DD} OR V _{CC}	V _{DD} OR V _{CC}	NO
	UB/SW	0	0	NO
	UB/UW	0	V _{DD} OR V _{CC}	NO

V_{PP} = 8~9V FOR G_{ox}=32A (0.18um) OR 5-7 FOR G_{ox}=20A, OR 3~4.5 V
FOR 10-15A (5 TO 10A THINNER THAN NORMAL STANDARD GATE OXIDE).
V_{DD} = I/O VOLTAGE 3.3V OR 2.5V
V_{CC} = 1.8V FOR 0.18um AND 1.2V FOR 0.13um

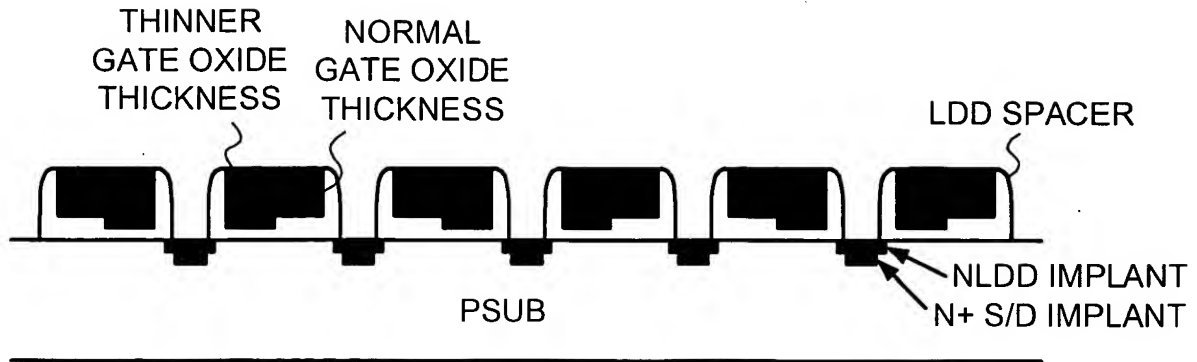
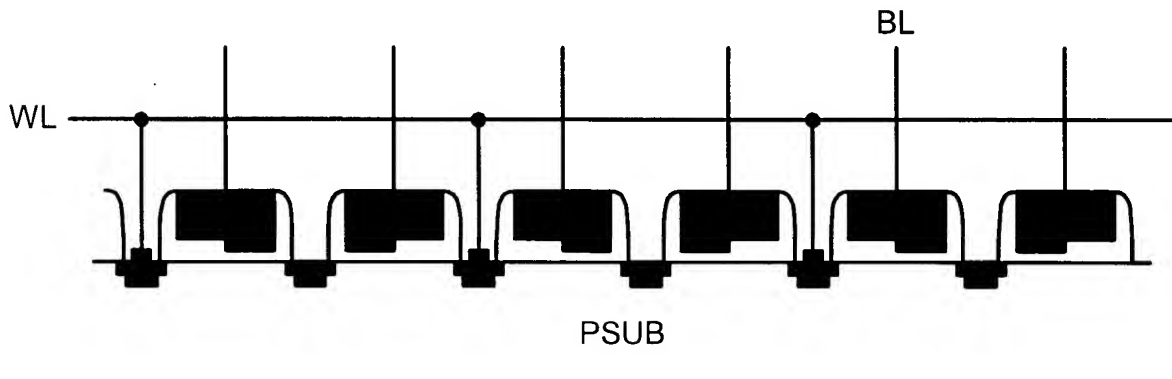
FIGURE 18

**FIGURE 19**

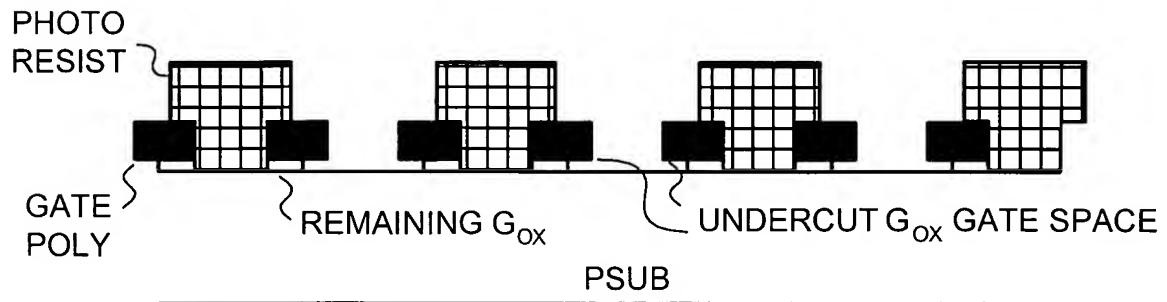
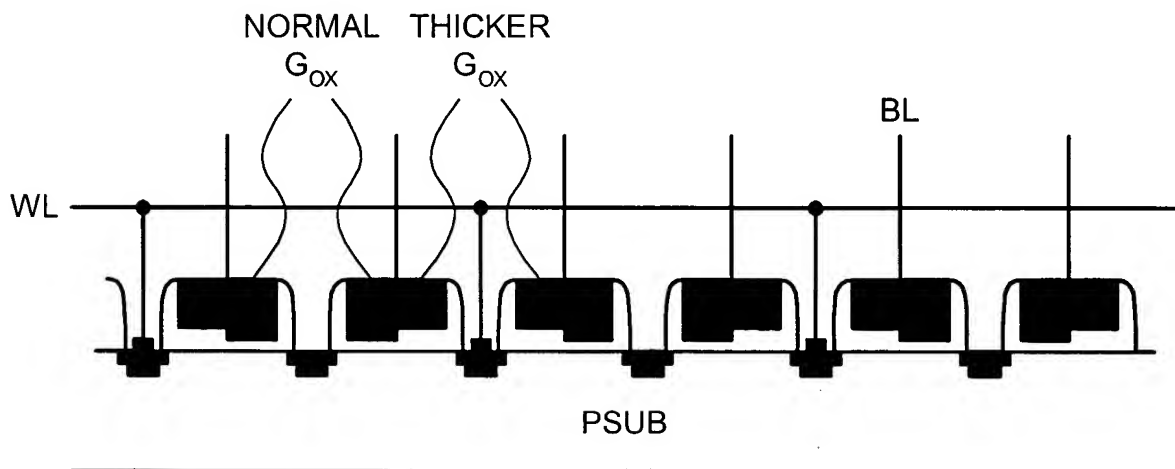
STEP 1:

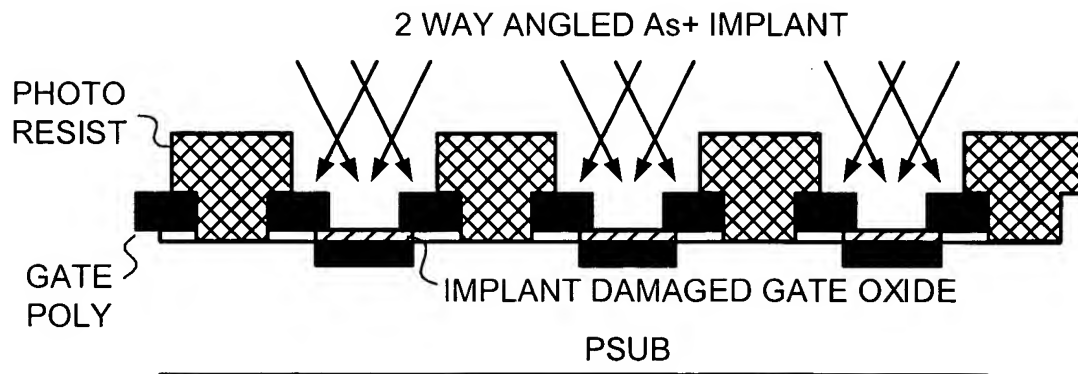
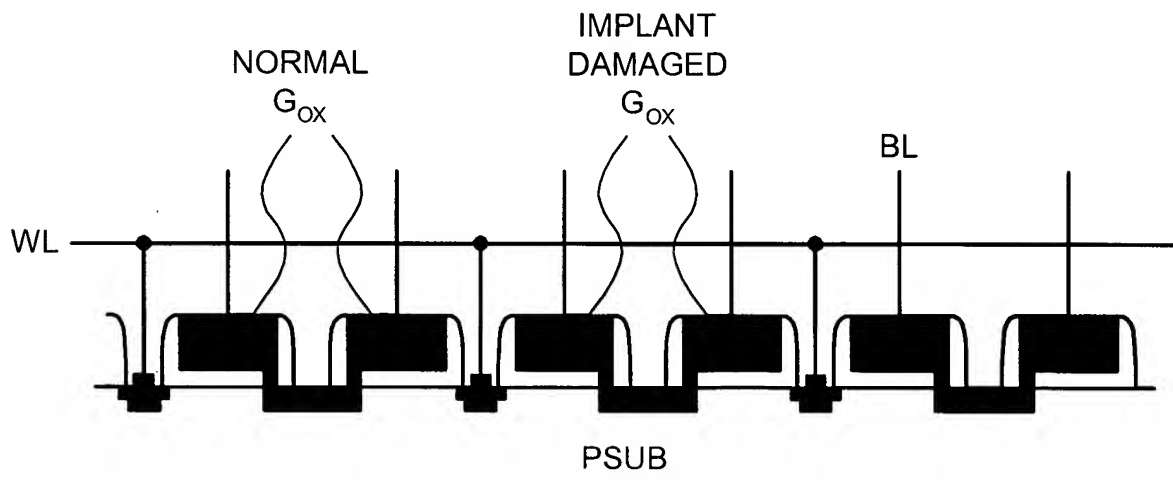
**FIGURE 20****FIGURE 21**

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**FIGURE 22****FIGURE 23**

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**FIGURE 24****FIGURE 25**

**FIGURE 26****FIGURE 27**